

Tuesday Keynote
**High-Performance, Scalable, General-Purpose Processors to
Accelerate High-Throughput Networking and Security
Applications**



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Abstract: As an example of modern, high-throughput embedded applications, network providers are evolving from proprietary hardware to standard, general-purpose servers (Networking Function Virtualization, or NFV). But then the challenge is to achieve sufficiently high performance to meet current and future requirements. A solution is offload acceleration. Given the trend to more flexible and higher-level networking and security functions, notably Software Defined Networking (SDN), a programmable solution is necessary. In order to leverage existing software components and skills, any solution must embrace standard tools and runtime environments. To provide high performance, both many general-purpose CPU cores and dedicated high-speed I/O hardware are required. Enabling all this in a power-efficient implementation requires a high-performance scalable interconnect and system design. As an example, we present Titera's TILE-Gx processors, scaling today from 9 to 72 cores, their architecture, and some performance and power results.

Biographical Sketch: Richard Schooler has more than 20 years of experience in technical leadership and engineering management in the software industry, primarily in programming language implementation, program transformation, and performance optimization. Before coming to Titera, he was Director of Windows Build for Microsoft Corporation. Mr. Schooler has served as a Technical Director at VERITAS Software, Vice President of Technology at Geodesic Systems, the Chief Technology Officer for InCert Software, and in project management and software engineering roles at Hewlett Packard, Bolt Beranek & Newman Advanced Computers, and Intermetrics. He has been granted five patents and has published technical papers in compiler implementation and program optimization. Mr. Schooler holds a BS in Computer Science and Mathematics and a MS in Computer Science from the Massachusetts Institute of Technology.