Industry Panel:
System-Level Design and High-Level Synthesis

Moderator:
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Hardware Synthesis Background

• **High-level synthesis is an old research topic**
  - Dating back to 1980s and early 1990s [VHDL]
  - 1\textsuperscript{st} gen: Synopsys Behavioral Compiler (1994-2004)

• **Resurrected as C-based hardware design**
  - Commercial experimentation

• **Recent expansion into (electronic) system-level (ESL)**
  - Beyond a single block, SoCs from concurrent “C”
  - Renewed interest in academia [LegUp, AutoESL, GAUT, …]
  - Commercial adoption?
Questions for the Panel

• What works and what doesn’t? And why?
  • Areas of commercial adoption?
  • Strengths and weaknesses of current solutions

• What is the trajectory for the future?
  • Widespread adoption or limited to niche applications?
  • Evolution potential and growth directions

• (Academic) research needs?
  • Mature field or fundamental challenges?
  • Short- and long-term needs

➢ User and tool vendor perspectives
Speakers

1. Yatin Hoskote (Intel)
   • Director of System-on-Chip Technology and IP, Intel Labs

2. Rishiyur S. Nikhil (Bluespec)
   • Co-founder and CTO

3. Andres Takach (Calypto)
   • Senior Architect