HIGH LEVEL DESIGN AND SYNTHESIS

Yatin Hoskote
Intel labs
ESWEEK Sept 2013

Acknowledgements: SoC Technology and IP, Design Technology Solutions

HLD and HLS at Intel

- Multiple teams using HLS
- Typically see 3X productivity gains for similar QoR
  - Algorithmic designs
- Sample results:

	Design A	Design B	Design C
QoR improvement	+7%	0%	+20%
Design TAT	3X	2X	2X
Validation TAT	7-10X	4X	5X
Simulation improvement	33X	10-30X	10X+

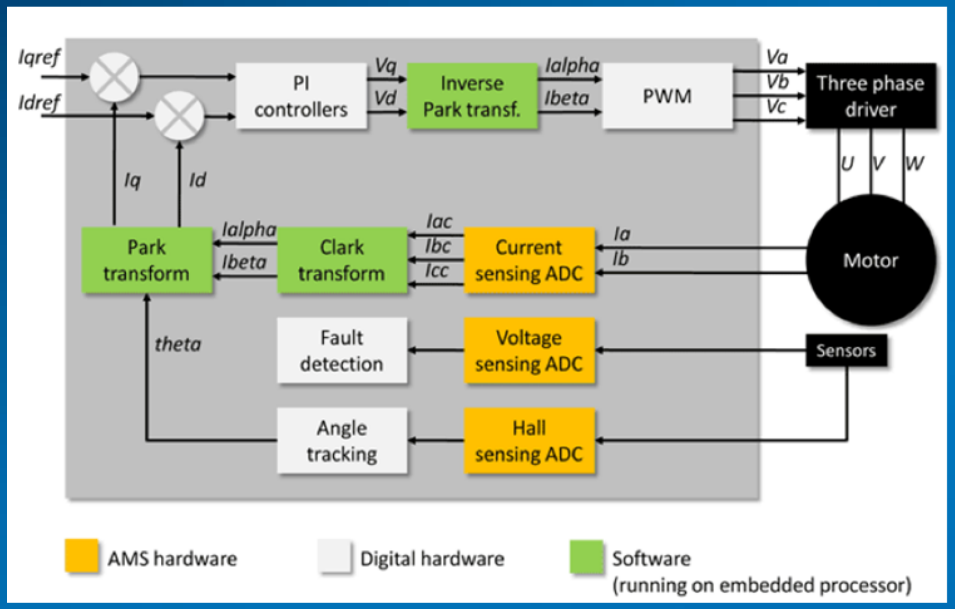
HLD and HLS at Intel

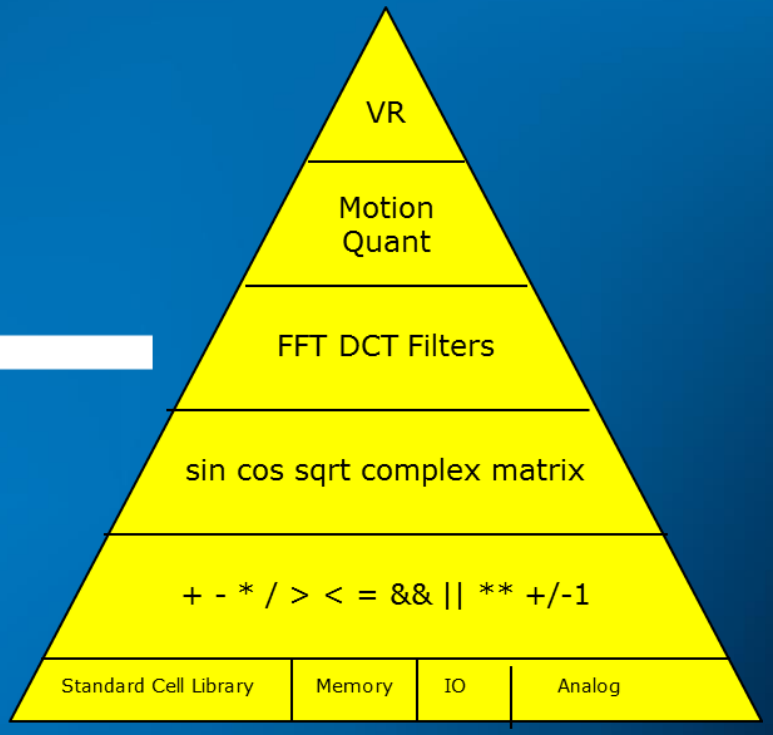
- Some barriers to adoption for HLS
  - Lack of SystemC expertise in users
  - Steep learning curve on the tools
  - Technology advanced but methodology needs work
  - Integration into existing design flow

Other HLD efforts:

- Use of virtual platforms for software development
- High level models for functional validation
- Performance verification uses custom models

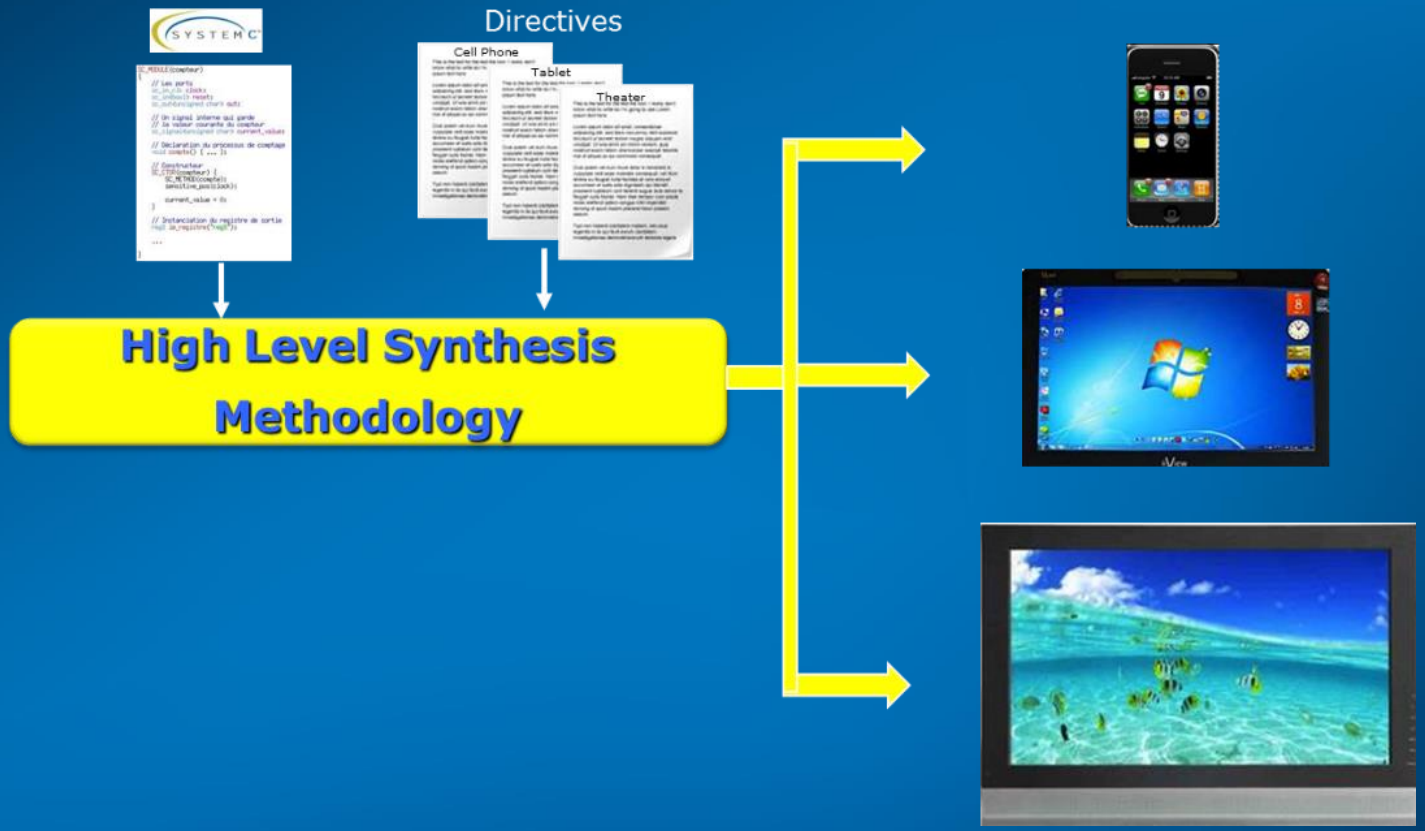
SystemC SOC / IP Model



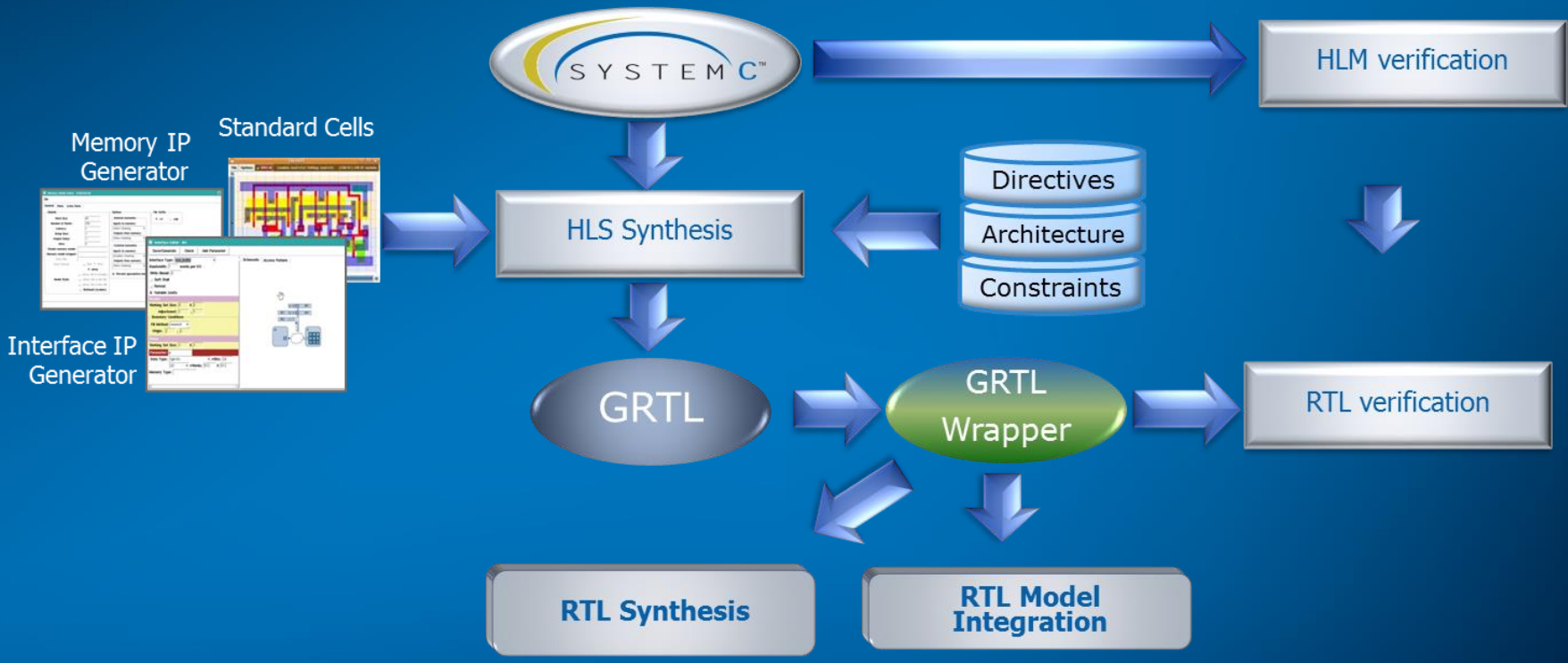


HLS Algorithmic Pyramid

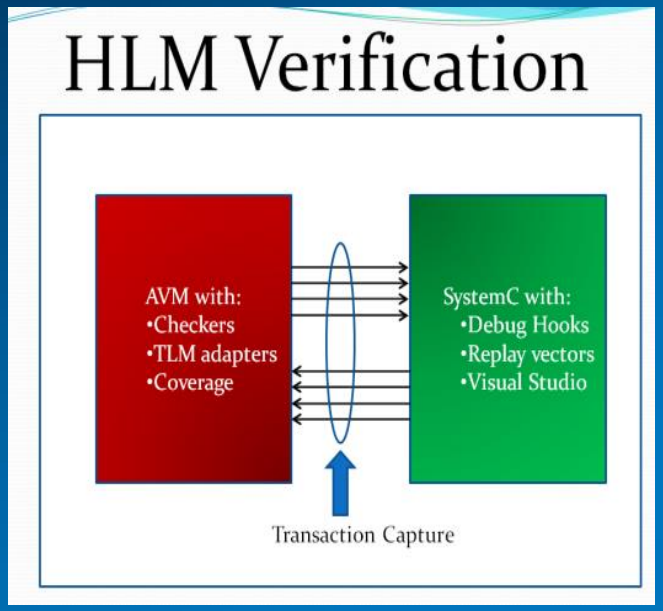
SYSTEMC DESIGN ENV AND DESIGN AIDS

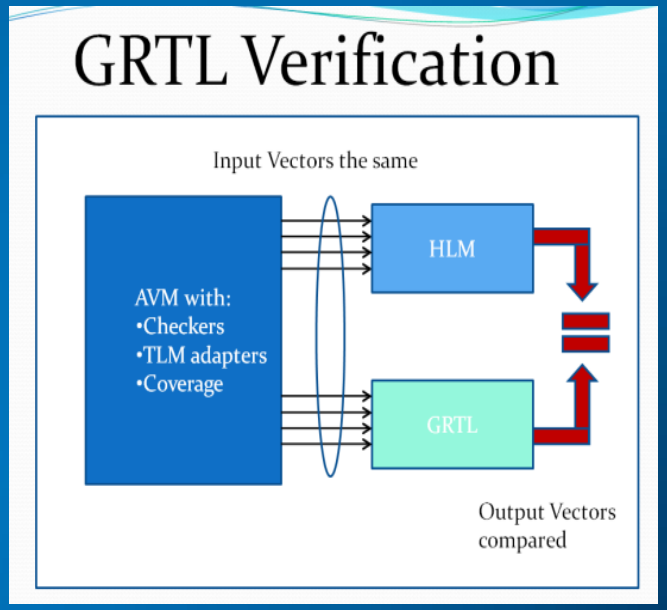


STANDARDIZATION ACROSS TOOLS, LANGUAGES

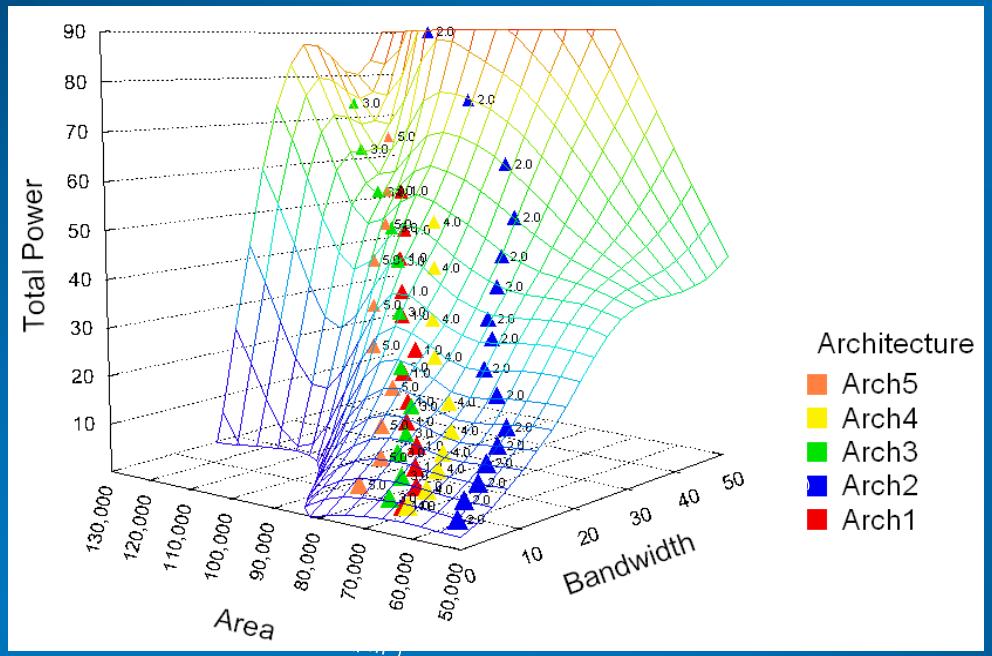


INTEGRATION INTO FLOWS

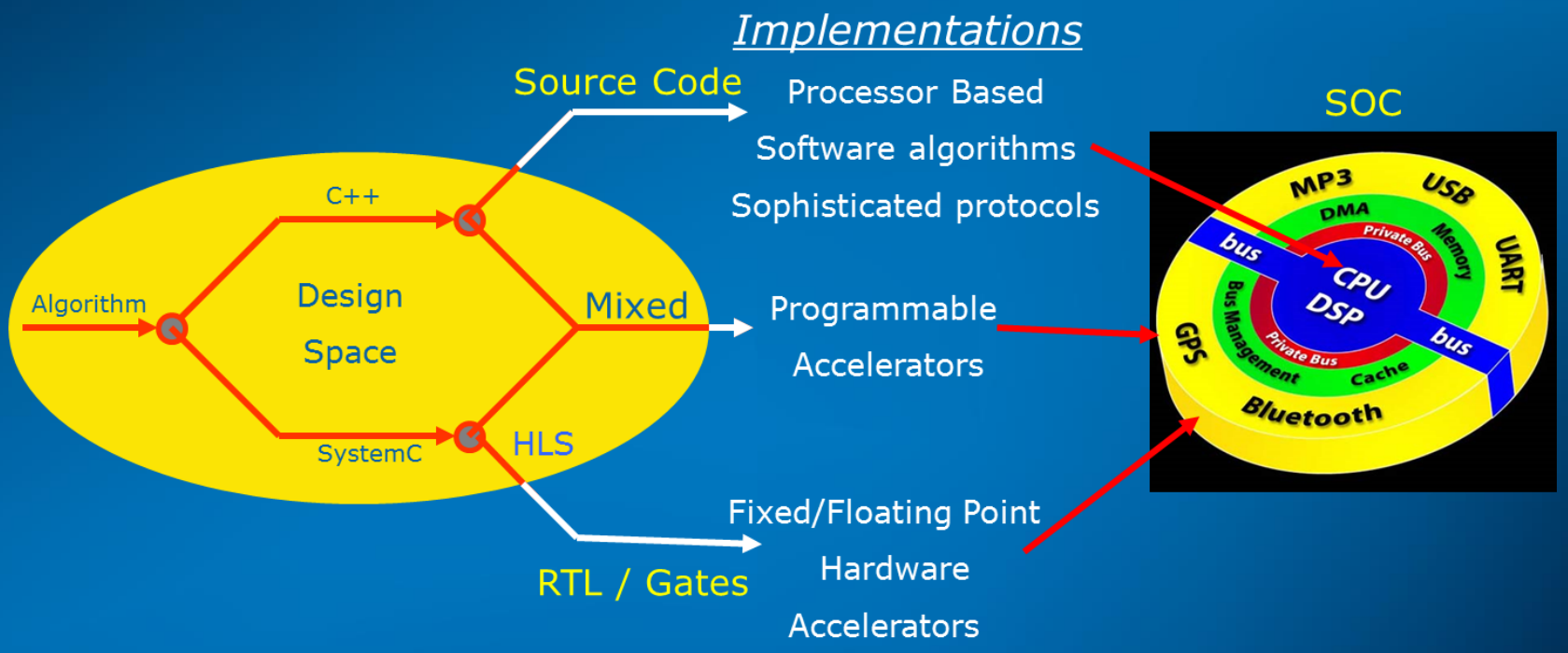




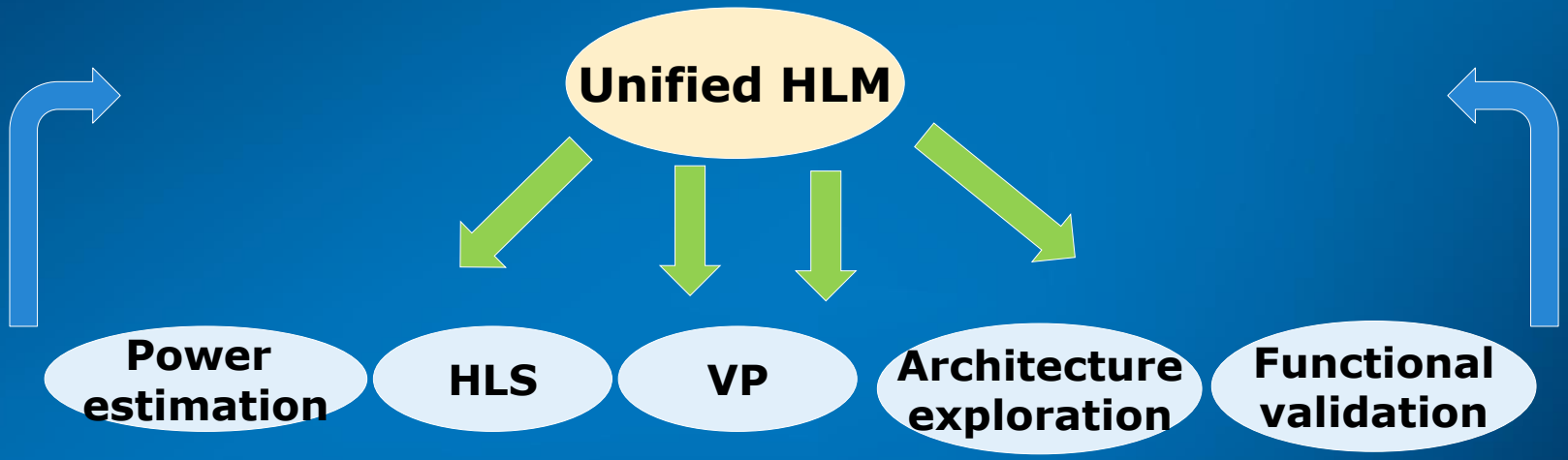
EQUIVALENCE VERIFICATION, SYSTEMC FV AND VALIDATION



EARLY ESTIMATION ACCURACY: AREA, PERFORMANCE, POWER



CO-DESIGN SUPPORT, MEMORY ANALYSIS ARCH EXPLORATION



SINGLE SOURCE MODELS

THANK YOU