



CODES+ISSS 2015: Call for Papers

The International Conference on Hardware/Software Codesign and System Synthesis is the premier event in the design, modeling, analysis, and implementation of modern embedded systems, from system-level specification and optimization to hardware/software implementation. The conference is a forum for active discussions on various topics of current and future importance to designers and researchers. The program of the conference brings together the latest and the best in academic and industrial research and development. High-quality original papers will be accepted for oral presentation followed by interactive poster sessions. CODES+ISSS 2015 is part of the [Embedded Systems Week 2015](#).

Program chairs:

[Gabriela Nicolescu](#), École Polytechnique de Montréal, Canada.

[Andreas Gerstlauer](#), The University of Texas At Austin, USA

Areas of Interest

CODES+ISSS invites contributions on specification, modeling, design, analysis, and implementation of embedded systems. The conference covers a wide range of design issues and applications relevant to important embedded system quality metrics including performance, cost, power consumption, reliability, security, and usability. The following relevant areas are representative but not exhaustive. We welcome submissions on novel solutions, new challenges, and emerging technologies in all these areas:

Track 1) Hardware/software co-design - Specification and refinement, design representation, system synthesis, partitioning, hardware-software interaction, design space exploration, reconfigurable design, and model-based design.

Track 2) Domain and application-specific design techniques - Analysis, design, and optimization techniques for multimedia, medical, automotive, security, and other specialized application domains, cyber-physical systems.

Track 3) Embedded software - Compilers, memory management, virtual machines, scheduling, operating systems, realtime support, fault-tolerance, and middleware.

Track 4) Embedded systems architecture - Architecture and micro-architecture design, exploration and optimization including application-specific, storage systems, memory and communication, networks-on-chip.

Track 5) Large-scale system architecture - Multi-cores, GP-GPUs, heterogeneous systems, data centers, cloud computing, sensor networks.

Track 6) Simulation, validation and verification - Hardware/software co-simulation, verification and validation methodologies, formal verification, hardware-accelerated simulation, test methodology, design for testability, specification languages/models, and benchmarks.

Track 7) Power-aware systems - Power- and energy-aware system design and methodologies ranging from low-power embedded systems to energy-efficient large scale systems such as Green IT and Smart Grid.

Track 8) Industrial practices and case studies - Practical impact on current and/or future industries with applications of the state-of-the-art methodologies and tools in various application areas including wireless, networking, multimedia, automotive, medical systems, etc.

Submission Information

Papers must represent original work, not published or submitted for publication in other forums. A blind review process will be enforced. Authors must not reveal their identity directly or indirectly. Papers must be in PDF format and should not exceed **10 pages** in ACM two-column format (9pt on 8.5"x11" letter size paper). For formatting instructions and templates, visit the [ACM web site](#). Of note, 10 pages is an upper limit. Authors are encouraged to submit shorter papers if this better fits the nature and content of the paper. Formal proceedings will be published on CD-ROM and online (Copyright held by ACM and IEEE).

Important Dates

Abstract Submission

March 23, 2015 (11:59 pm GMT-12)

Full Paper Submission

March 30, 2015 (11:59 pm GMT-12)
(Firm deadline)

Notification of Paper Acceptance

June 08, 2015

Camera-ready version

July 13, 2015

Conference

October 04-09, 2015